Reg No.:_____ 00000CS405121902 Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh semester B.Tech examinations (S), September 2020

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1 With neat sketch differentiate explicit and implicit parallelism. (4)

2 Explain COMA model for Multiprocessor Systems. (4)

3 Define a) Instruction issue latency b) Instruction issue rate. (4)

4 Explain the significance of multiport memory. (4)

5 How hardware synchronization can be achieved in a multiprocessor system. (4)

6 Explain different message routing schemes. (4)

7 What is meant by pipeline stalling? (4)

8 Differentiate between Carry save adder (CSA) and Carry propagation adder (CPA). (4)

9 Suggest different methods to overcome asynchrony problem. (4)

10 Explain distributed caching. (4)

PART B

Answer any two full questions, each carries 9 marks.

11 a) Define Amdahl's Law. (3)

b) Consider the execution of an object code with 200,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. (6)

Instruction type	**CPI**	**Instruction mix**
Arithmetic and logic	1	56%
Load/store with cache hit	2	22%
Branch	4	10%
Memory reference with cache miss	8	12%

Calculate the average CPI, MIPS rate and Execution time.

12 a) Compare RISC and CISC scalar processor architectures. (4)

b) Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics: (5)

Memory Level	Access time	Capacity	Cost/Kbyte
Cache	t1=20ns	s1=512Kbytes	c1=$1.30
Main Memory	t2=905ns	s2=32Mbytes	c2=$0.2
Disk array	t3=5ms	s3=40Gbytes	c3=$0.0003

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

(i) Calculate the effective access time.

(ii) Calculate the total memory cost.

13 a) State and explain Bernstein's conditions for parallelism? (3)

b) Detect parallelism in the following code using Bernstein's conditions. Assume there are sufficient numbers of resources available. (6)

P1: C=D*E

P2: M=G+C

P3: A=B+C

P4: C=L+M

P5: F=G/E

PART C

Answer any two full questions, each carries 9 marks.

14 a) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation π1=(0,6,3,2,5)(1,4). Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

b) Draw the two state transition graphs for a cache block using write -invalidate write -through snoopy bus protocol. (3)

15 a) With suitable diagram explain different flow control strategies for resolving a collision between two packets. (4)

b) Consider the following pipeline reservation table. (5)

	1	2	3	4
S1	X			
S2		X		X
S3			X	

i) What are the forbidden latencies?

ii) Draw the transition diagram.

iii) List all the simple cycles and greedy cycles.

iv) Determine the optimal constant latency cycle and minimal average latency (MAL).

v) Let the pipeline clock period be τ=10ns. Determine the throughput of the pipeline.

16 a) Compare full map directories with limited directories. (4)

b) Explain E-cube routing. Consider a 64 -node hypercube network. Based on E-cube routing algorithm, show how to route a message from 101101 to 011010. Find all intermediate nodes on routing path. (5)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Explain the importance of Tomasulo's algorithm for dynamic instruction scheduling. (6)

b) Describe the various mechanisms for improving the performance of instruction pipeline. (6)

18 a) Explain various latency hiding techniques. (8)

b) Differentiate between static and dynamic data flow computers. (4)

19 a) Explain various branch prediction techniques. (6)

b) With suitable diagrams explain ETL/EM-4 architecture. (6)

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