

Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY**  
SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

**Course Code: CS405**

**Course Name: COMPUTER SYSTEM ARCHITECTURE**

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer all questions, each carries 4 marks.*

- |    |   | Marks |
|----|---|-------|
| 1  | With a neat sketch, explain the architecture of a vector supercomputer.   | (4)   |
| 2  | Explain implicit and explicit parallelism in parallel programming   | (4)   |
| 3  | Compare the characteristics of CISC and RISC Architectures  | (4)   |
| 4  | Differentiate between crossbar network and multiport memory.  | (4)   |
| 5  | How does cache inconsistency occur in caches due to process migration and I/O?  | (4)   |
| 6  | Differentiate between store and forward and wormhole routing  | (4)   |
| 7  | What are the possible hazards that can occur between read and write operations in an instruction pipeline?  | (4)   |
| 8  | Determine the frequency of the pipeline if the stage delays are $\tau_1 = 3\text{ns}$ , $\tau_2 = \tau_3 = 5\text{ns}$ and $\tau_4 = 8\text{ns}$ and the latch delay is 1 ns. | (4)   |
| 9  | Distinguish between static dataflow computers and dynamic dataflow computers.   | (4)   |
| 10 | What are the four context switching policies for multithreaded architecture?  | (4)   |

**PART B**

*Answer any two full questions, each carries 9 marks.*

- 11 a) Explain Flynn's classification of computer architecture (4)
- b) A 40 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts:

Instruction Type	Instruction count	Clock cycle count
Integer Arithmetic	35000	1
Data Transfer	20000	2
Floating point	15000	2
Control Transfer	6000	2

Determine the effective CPI, MIPS rate and execution time for this program. (5)

- 12 a) Explain the terms (i) Hit Ratio (ii) Effective Access Time with proper (3)

equations

- b) Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=25$ ns	$s_1=512$ Kbytes	$c_1=\$1.25$
Main Memory	$t_2=903$ ns	$s_2=32$ Mbytes	$c_2=\$0.2$
Disk array	$t_3=4$ ms	$s_3=39.8$ Gbytes	$c_3=\$0.0002$

Hit ratio of cache memory is  $h_1=0.98$  and a hit ratio of main memory is  $h_2=0.9$ .

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost. (6)
- 13 a) Explain the role of compilers in exploiting parallelism (3)
- b) Explain VLIW architecture. Also explain pipelining in VLIW processors. (6)

### PART C

*Answer any two full questions, each carries 9 marks.*

- 14 a) Draw the state transition graph for a cache block using Goodman's write-once protocol for cache coherence. (3)
- b) Design an 8 input omega network using 2X2 switches as building blocks. (6)  
Show the switch settings for the permutation  $\pi_1=(0,6,4,7,3)(1,5)(2)$ . Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context.
- 15 a) Differentiate between synchronous and asynchronous model of linear pipeline processors. (3)
- b) Consider the following pipeline reservation table:

	1	2	3	4
S1	X			X
S2		X		
S3			X	

- i) What are the forbidden latencies?
- ii) Draw the transition diagram.
- iii) List all the simple cycles and greedy cycles.
- iv) Determine the optimal constant latency cycle and minimal average latency (MAL)

- v) Let the pipeline clock period be  $\tau=20\text{ns}$ . Determine the throughput of the pipeline. (6)
- 16 a) Explain full-map directory based protocol. (4)
- b) What do you mean by dimension order routing? Consider a 16 node hypercube network. Based on E-cube routing algorithm, show how to route a message from 0010 to 1001. Find all intermediate nodes on routing path. (5)

**PART D**

*Answer any two full questions, each carries 12 marks.*

- 17 (a) Explain the Tomasulo's algorithm for the dynamic instruction scheduling. (5)
- (b) Explain the concept of in-order issue and out-of-order issue with respect to superscalar processor. (7)
- 18 a) Explain any three latency hiding techniques used in distributed shared memory multi computers. (9)
- b) Write a short note on fine-grain parallelism. (3)
- 19 a) Explain static branch prediction strategy and dynamic branch prediction strategy. (6)
- b) With a neat diagram explain the architecture of ETL/EM-4 dataflow architecture. (6)

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